IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES
(Attorney Docket № 13757US03)

In the Application of:

Amir Morad et al.

Serial No. 10/776,541

Electronically Filed on 06-SEPT-2011

Filed: February 10, 2004

For: SYSTEM AND METHOD FOR VIDEO AND AUDIO ENCODING ON A SINGLE CHIP

Examiner: Tung T. Vo

Group Art Unit: 2486

Confirmation No. 3126

REPLY BRIEF

MS: APPEAL BRIEF-PATENTS
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with 37 CFR 41.41, the Appellant submits this Reply Brief in response to the Examiner's Answer ("Answer") mailed on July 7, 2011. Claims 10-36 are pending in the present Application. The Appellant has responded to the Examiner in the Examiner's Answer, as found in the following Argument section.

As may be verified in the final Office Action dated November 16, 2010 ("Final Office Action"), claims 10-36 stand rejected under 35 U.S.C. § 103(a). *See* Final Office

Action at page 2. To aid the Board in identifying corresponding arguments, the Appellant has used the same headings in the Argument section of this Reply Brief as the headings found in the Appellant's corresponding Brief on Appeal. The Brief on Appeal has a date of deposit of May 16, 2011.

STATUS OF THE CLAIMS

Claims 10-36 were finally rejected. Pending claims 10-36 are the subject of this appeal.

ARGUMENT

I. CLAIMS 10-20 AND 24-33 ARE PATENTABLE OVER THE PROPOSED COMBINATION OF ADOLPH AND HINCHLEY

A. Independent Claims 10 and 24

The Appellant stands by the argument made in the corresponding section of the Brief on Appeal.

1. **Adolph Does Not Disclose** "*MULTIPLEXER CIRCUITRY THAT OPERATES IN A FIRST MODE AND A SECOND MODE, WHICH WHEN OPERATING IN THE FIRST MODE PRODUCES A FIRST MULTIPLEXED STREAM FROM FIRST COMPRESSED VIDEO, FIRST COMPRESSED AUDIO, SECOND COMPRESSED VIDEO, AND SECOND COMPRESSED AUDIO.*"

In response to Appellant's Brief on Appeal, the Examiner is using the following argument stated in the Answer:

> The examiner strongly disagrees with the appellant. It is submitted that Adolph clearly discloses which when operating in the first mode (MMUX of fig. 3) produces a first multiplexed stream (the output of EMUX of fig. 3) from first compressed video (VE1 of fig. 3), first compressed audio (AE1 of fig. 3), second compressed video (VE2 of fig. 3), and second compressed audio (AE2 of fig. 3); and which when operating in the second mode concurrently produces the first multiplexed stream (MUX1 of fig. 3, the MUX1 clearly produces the multiplexed from the VE1 and AE1 as considered the first multiplexed stream) from the first compressed video (VE1 of fig. 1) and the first compressed audio (VE1), and produces a second multiplexed stream (MUX2 of fig. 2, the MUX1 produces the second multiplexed stream) from the second compressed video (VE2 of fig. 3) and the second compressed audio (AE2 of fig. 3). *The appellant argued that the office is inconsistent interpretation of Adolph.*

See Answer at p. 38-39 (emphasis added). The Examiner then continues on p. 39 of the Answer with a citation from the 6/10/10 non-final Office Action and the 11/16/10 Final Office Action.

Initially, the Appellant points out that the citation from the 6/10/10 non-final Office Action and the 11/16/10 Final Office Action were used in the Brief on Appeal (pp. 9 and 11) not to point out that they are inconsistent with each other in interpreting Adolph (on the contrary, both the 6/10/10 and 11/16/10 Office Actions interpret Adolph in the same way). Instead, the Brief on Appeal (at e.g., pp. 9-12) pointed out that both the 6/10/10 and 11/16/10 Office Actions are *misinterpreting the teachings of Adolph in light of Appellant's recitations in claims 10 and 24.*

Both the 6/10/10 NFOA (p. 2) and 11/16/10 FOA (p. 5) identify the entirety of FIG. 3 of Adolph as teaching Appellants' claimed "audio/video encoder device," and *the portion of FIG. 3 labeled "EMUX" as teaching Appellant's claimed "multiplexer circuitry."* (Id.) The Examiner also interprets the "performing of MMUX" of FIG. 3 of Adolph as teaching Appellant's "first mode," and the "performing of MUX 1 and MUX 2" of FIG. 3 of Adolph as teaching Appellant's "second mode." (Id.) The Examiner then relies on that interpretation of Adolph, in asserting that cited aspects of only Adolph disclose Appellant's claimed "single-chip audio/video encoder device comprising, on a single integrated circuit: multiplexer circuitry that operates in a first mode and a second mode, which when operating in the first mode produces a first multiplexed stream from first compressed video, first compressed audio, second compressed video, and second compressed audio." (Id.)

The Examiner has specifically equated Adolph's EMUX (Fig. 3) to Appellant's "multiplexer circuitry". However, even though Adolph's EMUX uses three multiplexers (MUX1, MUX2, and MMUX), all of the three multiplexers always work concurrently, resulting in the generation of a **single** output (namely, the output of MMUX). This is also supported by the following citation from Adolph:

> The various (in the example of FIG. 3: two) programme data streams are then combined in a transport multiplexer MMUX to form a transport data stream in accordance with the MPEG2 system specification...

(*See* Adolph, col. 4, lines 38-41; emphasis added). Put another way, **the MMUX (i.e., the alleged "multiplexer circuitry") operates only in *one* mode and generates only a *single* output**.

In p. 41 of the Answer, the Examiner uses the following chart:

Appellant's Claim	ADOLPH TEACHES
IN THE FIRST MODE: **multiplexer circuitry** that operates when operating in **the first mode** produces **a first multiplexed stream** from **first compressed video, first compressed audio, second compressed video**, and **second compressed audio**	MMUX OF FIG. 3 using four components as VE1, AE1, VE2, and AE2 of fig. 3
IN THE SECOND MODE: concurrently produces **the first multiplexed stream** from **the first compressed video** and **the first compressed audio**	MUX1 OF FIG. 3 using two components as VE1 and AE1 of fig. 3
IN THE SECOND MODE: produces **a second multiplexed stream** from **the second compressed video** and the **second compressed audio**	MUX 2 OF FIG. 3 using two components as VE2 and AE2 of fig. 3

(Annotations added by Appellant). The above chart, however, is misleading and does not support the Examiner's arguments. **As can be seen from the annotated chart, the MMUX of Adolph's Fig. 3 is equated to Appellant's "multiplexer circuitry". Additionally, Appellant's claims 10 and 24 require that the same "multiplexer circuitry" produces the multiplexed streams in *both* the First and Second modes. However, as seen from the above chart, the Examiner is alleging**

that MUX1 and MUX2 produce the multiplexed streams in the Second mode. Obviously, MUX1 and MUX2 are not the same as the MMUX module (they are both part of it).

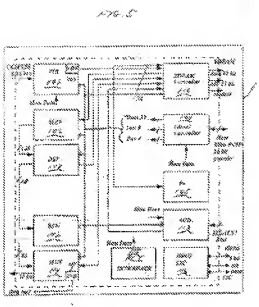
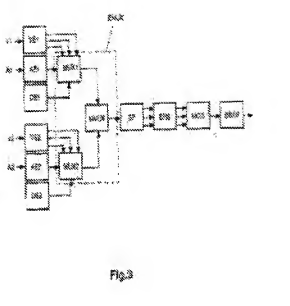
Therefore, Adolph does not (and cannot) disclose "multiplexer circuitry that operates in a first mode and a second mode, which when operating in the first mode produces a first multiplexed stream from first compressed video, first compressed audio, second compressed video, and second compressed audio; and which when operating in the second mode concurrently produces the first multiplexed stream from the first compressed video and the first compressed audio, and produces a second multiplexed stream from the second compressed video and the second compressed audio," as recited in Appellant's claims 10 and 24.

2. **Adolph Does Not Disclose** *"WHEREIN THE DEVICE TRANSMITS THE FIRST MULTIPLEXED STREAM TO CIRCUITRY EXTERNAL TO THE DEVICE VIA A FIRST OUTPUT OF THE DEVICE" AND "WHEREIN THE DEVICE TRANSMITS THE SECOND MULTIPLEXED STREAM TO CIRCUITRY EXTERNAL TO THE DEVICE VIA A SECOND OUTPUT OF THE DEVICE"*

In response to Appellant's Brief on Appeal, the Examiner is using the following argument stated in the Answer:

> The examiner strongly disagrees with the appellant. Adolph teaches the first multiplexed stream is performed by MUX1 of figure 3 in the second mode, and the second multiplexed stream is performed by MUX2 of figure 3 in the second mode. The first multiplexed stream is transmitted to circuitry external to the device by the MMUX, SP, ERS, MOD, and BBRF of figure via a first output (the output MUX 1) of the device, and the second multiplexed stream is transmitted to circuitry external to the device by the MMUX, SP, ERS, MOD, and BBRF of figure via a first output (the output MUX 2) of the device.

See Answer at p. 42. The Examiner then uses the following chart to compare Appellant's FIG. 5 and Adolph's FIG. 3:

	
It is clear that the MUX 114 is outputting the first multiplexed stream and the second multiplexed stream to the circuitry external.	Adolph discloses the MMUX is outputting the first multiplexed stream from MUX1 and the second multiplexed stream from MUX2 to the circuitry external delivered by SP, ERS, MOD, and BBRF.

(*See* Answer, p. 43). The above chart, however, does not support the Examiner's arguments. More specifically, as seen in Fig. 3 of Adolph, **the EMUX has a single output (which is the same as the output of the MMUX), and even the entire device in Fig. 3 has a single output (e.g., output of BBRF module). In this regard, Adolph does not disclose at least two separate outputs (at least a first output and a**

second output of the device) to external circuitry. Even assuming for the sake of argument that Appellant's "first multiplexed stream" and "second multiplexed stream" are the outputs of the MUX1 and MUX2 multiplexers, respectively, the Examiner's argument is still deficient since both of the MUX1 and MUX2 outputs are communicated to the MMUX and not to external circuitry.

Therefore, Adolph does not (and cannot) disclose "wherein the device transmits the first multiplexed stream to circuitry external to the device via a first output of the device" and "wherein the device transmits the second multiplexed stream to circuitry external to the device via a second output of the device," as recited in Appellant's claims 10 and 24.

3. **Hinchley Does Not Disclose** *"CONTROL CIRCUITRY THAT SYNCHRONIZES THE MULTIPLEXING CIRCUITRY, THE FIRST ENCODER, AND THE SECOND ENCODER".*

In response to Appellant's Brief on Appeal, the Examiner is using the following argument stated in the Answer:

> Hinchley discloses multiplexer circuitry (200 of fig. 2, note the stream processor, 200 of fig. 2, comprises the MUX LOGIC (750 of fig. 7) is compliant with MPEG2 standard, which has the same functions as multiplexing circuitry as disclosed above of the present invention) that operates in a first mode and a second mode (MUX logic (750 of fig. 7) performs multiplexing operations that encompass a first mode and second mode). Since Hinchley discloses the MUX logic (750 of fig. 7) have multiplexing operations as modes with recognized standards such as MPEG2, col. 6, lines 12-26, so the MUX logic performs when operating in the first mode produces a first multiplexed stream from first compressed video, first compressed audio, second compressed video, and second compressed audio; and when operating in the second mode concurrently produces the first multiplexed stream from the first compressed video and the first compressed audio, and produces a second multiplexed stream from the second compressed video and the second compressed audio, which is the same the multiplexing circuitry, 114 of fig. 5, of the present

> invention as disclosed in the specification, [0040], [0061], [0063], and [0064].

See Answer at p. 45. The Examiner, at p. 43-44 of the Answer, has alleged that Appellant's "multiplexing circuitry" is described only in several paragraphs of Appellant's disclosure. The Appellant respectfully disagrees with such limited description of Appellant's "multiplexing circuitry", and submits that the Examiner should, instead, look at Appellant's entire disclosure (including the cited and incorporated by reference related applications) for explanation of how various elements and structures (including the "multiplexing circuitry") operate.

With this in mind, the Appellant now turns to the specific arguments listed in p. 45-47 of the Answer. In the above citation from p. 45 of the Answer, the Examiner refers for support to Hinchley and alleges that the MUX logic (750 in Fig. 7) operates in a first mode and a second mode. The Appellant disagrees and submits that there is absolutely no support in Hinchley for such characterization of the MUX logic 750 by the Examiner. Hinchley, at col. 6, lines 15-18, discloses that the MUX logic 750 only discloses conventional multiplexing operations in accordance with recognized standards (such as MPEG2) to generate a combined multimedia stream. Nothing in this citation of Hinchley (or any other remaining citation) discloses that the MUX logic 750 operates in a plurality of modes (e.g., a first mode and a second mode), where different multiplexed streams are output during for each corresponding mode.

The Examiner also uses a "comparison chart" in p. 46 of the Answer, and then concludes without any explanation or analysis whatsoever that "Hinchley's MUX logic (750 of fig. 7) has the same functions (MPEG2 standards) as Multiplexing processor

(114 of fig. 5) of the present invention". The Appellant disagrees and points out that Examiner's above allegation amounts to no more than a conclusory statement, which fails to provide the "explicit analysis" required by MPEP §2142 to explain why the cited art (Hinchley) is interpreted in this way.

A review of Hinchley shows that the entirety of Hinchley fails to make any mention of "synchronization." Cited element "250" of Hinchley, which has been identified by the Examiner as teaching Appellant's element "control circuitry," is identified by Hinchley as "multimedia processor 250." (*See* Hinchley at col. 3, line 50). According to Hinchley, "[m]ultimedia processor 250 is preferably a Digital Signal Processing (DSP) core which is designed to perform conventional multimedia operations as well as the specialized functions in accordance with the present invention." Id. at 3:65-4:2. Nothing in Hinchley teaches or suggests that the "multimedia processor 250" "synchronizes" anything, let alone synchronizing the "multimedia encoder 208" and "stream processor 200" of Fig. 2, which have been identified by the Examiner as teaching Appellant's claim elements "first/second encoder" and "multiplexer circuitry." Hinchley merely teaches that the "multimedia engine 250" adjusts a "data rate" of only an encoder, but says nothing about "synchronization." Id. at 6:13-8:44. Indeed, adjusting a "data rate" is quite different from "synchronization" (as claimed), and Hinchley fails to make any mention of "synchronization" of anything in its entirety, let alone of the elements and the manner claimed. **NOTE: The Examiner's Answer has not provided any substantive response to the above arguments related to the alleged disclosure of "control**

circuitry" in Hinchley (the above arguments also appear in pages 18-19 of the Brief on Appeal).

Accordingly, clam 10 is also patentable because the proposed combination of Adolph and Hinchley fails to disclose or suggest "control circuitry that synchronizes the multiplexing circuitry, the first encoder, and the second encoder," as required by claim 10. Therefore, based at least upon the above, Appellants respectfully submit that the Examiner has not shown that the cited art teaches all aspects of Appellants' claim 10, that the Examiner has not established a prima facie case of obviousness, and that claim 10 is allowable over the cited art.

IV. CLAIMS 10-12, 15-16, 20, 24-25, 28-29, AND 33 ARE PATENTABLE OVER THE PROPOSED COMBINATION OF KRISHNAMURTHY AND ADOLPH

A. Independent Claims 10 and 24

1. **Krishnamurthy Does Not Disclose "***MULTIPLEXER CIRCUITRY THAT OPERATES IN A FIRST MODE AND A SECOND MODE, WHICH WHEN OPERATING IN THE FIRST MODE PRODUCES A FIRST MULTIPLEXED STREAM FROM FIRST COMPRESSED VIDEO, FIRST COMPRESSED AUDIO, SECOND COMPRESSED VIDEO, AND SECOND COMPRESSED AUDIO.***"**

In response to Appellant's Brief on Appeal, the Examiner is using the following argument stated in the Answer:

> The examiner respectfully disagrees with the appellant. It is submitted that Krishnamurthy teaches a single-chip audio/video encoder device (fig. 3) that comprises first encoder circuitry (306, ENC1 of fig. 3), second encoder circuitry (306, ENCn of fig. 3), multiplexer circuitry (308 of fig. 3), controller circuitry (304 of fig. 3), and at least one bus interface (302 of fig. 3); wherein the first encoder circuitry (306, ENC1 of fig. 3) comprises: a first video encoder (302 of fig. 3), a first audio encoder (322 of fig. 3), a

> first motion estimation processor (MPEG-2 encoder, 320 of fig. 2, would obviously comprise a motion estimation processor); wherein the second encoder circuitry (306, ENCn of fig. 3) comprises: a second video encoder (320 of fig. 3), a second motion estimation processor (320 of fig. 3, ENCn, MPEG-2 encoder obviously comprise a motion estimation processor), a second audio encoder (322, ENCn of fig. 3); wherein the multiplexer circuitry (308 of fig. 3) multiplexes the compressed video and audio outputs from the encoders (306 of fig. 3) to produce the multiplexed signal, and the multiplexed signal is transmitted to circuitry external to the device (col. 19, lines 50 52, note the circuitry would obviously be a serial output port).
>
> Krishnamurthy suggests models of encoders and multiplexer (fig. 3) will be useful for the advance allocation statistical multiplexer (e.g. 308 of fig. 3) that have mostly been developed for natural video and need modifications for game and web content. This is evidence to one skill in the art to use any suitable and conventional device to modify the statistical multiplexer (col. 15, lines 45-50).

See Answer at p. 52-53. The above is merely a repetition of the argument stated in p. 8 of the 6/10/10 Office Action. The Examiner has relied on Krishnamurthy (col. 20, lines 12-25) to teach Appellant's "first mode" and "second mode". However, Krishnamurthy at col. 20, lines 12-25 merely teaches a multi-channel mode, which relates not to operating modes that define video and audio content of multiplexed streams, but instead to transmission of statistical parameters of encoders.

The Examiner then alleges that Krishnamurthy, at col. 15, lines 45-50, provides reasons for modifying the statistical multiplexer in the manner suggested by the Examiner. However, Krishnamurthy, at col. 15, lines 45-50, relate to rate-distortion models (used for encoding) and the need for modification to these rate-distortion models (not to the multiplexer) "for game and web content." Therefore, Krishnamurthy,

at col. 15, lines 45-50, does not even relate to the multiplexer 308 and the above reasoning by the Examiner does not support the conclusion of obviousness.

In p. 53-54 of the Answer, the Examiner has specifically equated Adolph's EMUX (Fig. 3) to Appellant's "multiplexer circuitry". However, even though Adolph's EMUX uses three multiplexers (MUX1, MUX2, and MMUX), all of the three multiplexers always work concurrently, resulting in the generation of a **single** output (namely, the output of MMUX). This is also supported by the following citation from Adolph:

> The various (in the example of FIG. 3: two) programme data streams are then combined in a transport multiplexer MMUX to form a transport data stream in accordance with the MPEG2 system specification...

(*See* Adolph, col. 4, lines 38-41; emphasis added). Put another way, **the MMUX (i.e., the alleged "multiplexer circuitry") operates only in *one* mode and generates only a *single* output**.

In p. 54 of the Answer, the Examiner uses the following chart:

Appellant's Claim	ADOLPH TEACHES
IN THE FIRST MODE: **multiplexer circuitry** that operates when operating in **the first mode** produces **a first multiplexed stream** from **first compressed video, first compressed audio, second compressed video**, and **second compressed audio**	MMUX OF FIG. 3 using four components as VE1, AE1, VE2, and AE2 of fig. 3
IN THE SECOND MODE: concurrently produces **the first multiplexed stream** from **the first compressed video** and **the first compressed audio**	MUX1 OF FIG. 3 using two components as VE1 and AE1 of fig. 3
IN THE SECOND MODE: produces **a second multiplexed stream** from **the second compressed video** and the **second compressed audio**	MUX 2 OF FIG. 3 using two components as VE2 and AE2 of fig. 3

(Annotations added by Appellant). The above chart, however, is misleading and does not support the Examiner's arguments. **As can be seen from the annotated chart, the MMUX of Adolph's Fig. 3 is equated to Appellant's "multiplexer circuitry". Additionally, Appellant's claims 10 and 24 require that the same "multiplexer circuitry" produces the multiplexed streams in *both* the First and Second modes. However, as seen from the above chart, the Examiner is alleging**

that MUX1 and MUX2 produce the multiplexed streams in the Second mode. Obviously, MUX1 and MUX2 are not the same as the MMUX module (they are both part of it).

Therefore, neither Krishnamurthy nor Adolph (individually or in reasonable combination) disclose "multiplexer circuitry that operates in a first mode and a second mode, which when operating in the first mode produces a first multiplexed stream from first compressed video, first compressed audio, second compressed video, and second compressed audio," as recited in Appellant's claims 10 and 24.

2. **Krishnamurthy Does Not Disclose** *"WHEREIN THE DEVICE TRANSMITS THE FIRST MULTIPLEXED STREAM TO CIRCUITRY EXTERNAL TO THE DEVICE VIA A FIRST OUTPUT OF THE DEVICE" AND "WHEREIN THE DEVICE TRANSMITS THE SECOND MULTIPLEXED STREAM TO CIRCUITRY EXTERNAL TO THE DEVICE VIA A SECOND OUTPUT OF THE DEVICE"*

In response to Appellant's Brief on Appeal, the Examiner is using the following argument stated in the Answer:

> The examiner respectfully disagrees with the appellant. It is submitted that Krishnamurthy teaches the outputs from the stat -mux are transmitted to circuitry (coL19, lines 50-52, note the on-chip DMA will automatically move data from the TS output buffer of on-chip memory to the serial output port, this is evidence that the multiplexed compressed bitstreams are transmitted to the serial output port as circuitry) external to the device (306 and 308 of fig. 3). It is noted that the circuitry external to the device is well known in the art and is taught by Hinchley (Note the circuitry external (116 or 112 of fig. 1) to the device (120 of fig. 1, see also fig. 2).

See Answer at p. 58. The Examiner is apparently now relying for support on ***Hinchley***. However, the Appellant notes that the present 35 USC 103(a) rejection is based on the

combination of Krishnamurthy and Adolph (not Hinchley). At least for this reason, the Appellant submits that the above argument by the Examiner is moot.

> The Examiner also states the following:
>
> The appellant further argued that Krishnamurthy does not teach "a first output to circuitry external to the device", and "a second output to circuitry external to the device".
>
> The examiner respectfully disagrees with the appellant. It is submitted that Krishnamurthy teaches the multiplexer, 308 of fig. 3, for outputting the multiplexed bitstream to circuitry external to the device by the output port (342 of fig. 3); this indicates that the output of the multiplexed bitstream must be transmitted to circuitry external to the device such as a memory device or a communication device. It is noted that circuitry external from the single chip audio/video encoder device is well known in the art and is taught by Hinchley (figure 1, circuitry as 112 and 116, external to the device as 120).

See Answer at p. 58-59. The Examiner is again relying for support on ***Hinchley***. However, the Appellant notes that the present 35 USC 103(a) rejection is based on the combination of Krishnamurthy and Adolph (not Hinchley). At least for this reason, the Appellant submits that the above argument by the Examiner is moot.

In addition, Krishnamurthy "relates to the compression and transmission of video signals, and, in particular, to the compression and transmission of multiple compressed video streams over a single, shared communication channel." (Krishnamurthy at 1:15-19.) The Examiner seems to acknowledge this deficiency of Krishnamurthy (see 6/10/10 Office Action, p. 9) and mistakenly relies for support on Adolph. The deficiencies of Adolph in this regard are provided in greater detail at p. 25-26 of the Brief on Appeal.

3. **Hinchley Does Not Disclose** *"CONTROL CIRCUITRY THAT SYNCHRONIZES THE MULTIPLEXING CIRCUITRY, THE FIRST ENCODER, AND THE SECOND ENCODER".*

In response to Appellant's Brief on Appeal, the Examiner is using the following argument stated in the Answer:

> The examiner respectfully disagrees with the appellant. It is submitted that Krishnamurthy further teaches a Central Processing Unit (CPU) (304 of fig. 3) that is programmable to control all elements in the circuit board of figure 3, so the Central Processing Unit (CPU) (304 of fig. 3) would synchronize, coordinate, harmonize, or orchestrate operation of the first encoder circuitry (306 of fig. 3), the second encoder circuitry (306n of fig. 3), and the multiplexer circuitry (308 of fig. 3) in order for all circuit properly working.
>
> Krishnamurthy further discloses Computer systems in accordance with the present invention avoid PCI bus delay by using the built-in multi-channel Synchronized Serial Interface (SSI) ports of multiple Digital Signal Processors (DSPs), where each DSP performs video and audio encoder control, PES/TS layer multiplexing, and computation of statistical measurements of its corresponding video stream payload. The DSPs' on-chip memories may also eliminate the need for bitstream First-In, First-Out (FIFO) chips and some common SDRAM (Synchronized Dynamic Random Access Memory) chips (**col. 17, line 65-col. 18, line 8**). There is CPLD (Complex Programmable Logic Device) or FPGA (Field-Programmable Gate Array) based deframing firmware to split the video and audio data, and to reproduce the video synchronization signals for the MPEG2 video encoder chip (**col. 19, lines 18-22**), the above disclosure is evidence that the Krishnamurthy's controller circuitry synchronizes operation of the first encoder, the second encoder and the multiplexer circuit.

See Answer at p. 59-60 (emphasis added). The Examiner is relying for support on col. 17, line 65-col. 18, line 8 and col. 19, lines 18-22. However, Krishnamurthy, at col. 17, line 65-col. 18, line 8, simply states that the DSPs use SSI ports, which has nothing to do with the DSP itself performing any synchronization functions (e.g., synchronization of multiplexer circuitry with a plurality of encoders). Krishnamurthy, at

col. 19, lines 18-22, discloses reproducing of video synchronization signals for the MPEG2 video encoder chip, which, again, has nothing to do with the DSP itself performing any synchronization functions (e.g., synchronization of multiplexer circuitry with a plurality of encoders). Therefore, the Examiner's allegation that "the above disclosure is evidence that the Krishnamurthy's controller circuitry synchronizes operation of the first encoder, the second encoder and the multiplexer circuit" amounts to no more than a conclusory statement, which fails to provide the "explicit analysis" required by MPEP §2142 to explain why the cited art (Krishnamurthy) is interpreted in this way.

Accordingly, clam 10 is also patentable because the proposed combination of Krishnamurthy and Adolph fails to disclose or suggest "control circuitry that synchronizes the multiplexing circuitry, the first encoder, and the second encoder," as required by claim 10. Therefore, based at least upon the above, Appellants respectfully submit that the Examiner has not shown that the cited art teaches all aspects of Appellants' claim 10, that the Examiner has not established a prima facie case of obviousness, and that claim 10 is allowable over the cited art.

CONCLUSION

The Appellant submits that the pending claims are allowable in all respects. Reversal of the Examiner's rejections for all the pending claims and issuance of a patent on the Application are therefore requested from the Board.

The Commissioner is hereby authorized to charge additional fee(s) or credit overpayment(s) to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Respectfully submitted,

Date: 06-SEPT-2011

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